

PATENT APPLICATION

**ALTERNATIVE FLIP CHIP IN LEADED MOLDED PACKAGE
DESIGN AND METHOD FOR MANUFACTURE**

Inventor(s): Romel N. Manatad
1101 H. Cortes St.
Subangdaku, Mandaue City,
Cebu, Philippines, 6015
Citizenship: Philippines

**ALTERNATIVE FLIP CHIP IN LEADED MOLDED PACKAGE
DESIGN AND METHOD FOR MANUFACTURE**

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This patent application is a non-provisional patent application of
5 U.S. Patent Application No. 60/446,918, filed on February 11, 2003, which is herein
incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

[0002] A Flipchip in Leaded Molded Package (FLMP) is described in US
10 Patent Application No. 09/464,717. In a conventional FLMP package, the backside of
a silicon die is exposed through a window in a molding material. The backside of the
die can be in substantially direct thermal and electrical contact with a circuit substrate
such as a PC board.

[0003] When the FLMP package is made, a molding process is performed
15 after the die is attached to a leadframe structure. To keep the backside of the die clean
from mold bleed or mold flash, the package is designed so that no gap is present
between the mold cavity and the backside of silicon die. During manufacture, the die
is contacted by a mold tool upon mold tool clamping. Since the die is brittle and since
the package is thin, the potential for breakage of the die and disconnection between
the die and the leadframe is of concern.

20 **[0004]** Embodiments of the invention address these and other problems.

SUMMARY OF THE INVENTION

[0005] Embodiments of the invention are directed to semiconductor packages
and methods for making semiconductor packages.

25 **[0006]** One embodiment of the invention is directed to a method for making a
semiconductor package comprising: (a) molding a molding material around a
leadframe structure having a die attach region and a plurality of leads, wherein the die

attach region is exposed through a window in the molding material; and (b) after (a), mounting a semiconductor die to the die attach region using a flip chip mounting process.

5 **[0007]** Another embodiment of the invention is directed to a semiconductor package comprising: (a) a leadframe structure comprising a die attach region and plurality of leads; (b) a molding material molded around at least a portion of the leadframe structure, and wherein the molding material comprises a window; and (c) a semiconductor die mounted on the die attach region.

10 **[0008]** Another embodiment of the invention is directed to an electrical assembly comprising: a semiconductor package comprising (a) a leadframe structure comprising a die attach region and plurality of leads, (b) a molding material molded around at least a portion of the leadframe structure and wherein the molding material comprises a window, and (c) a semiconductor die comprising an edge mounted on the die attach region, wherein the semiconductor die is within the window, and wherein a
15 gap is present between the edge and the molding material; and a circuit substrate, wherein the semiconductor package is mounted to the circuit substrate.

[0009] These and other embodiments of the invention are described in further detail below.

BRIEF DESCRIPTION OF THE DRAWINGS

20 **[0010]** FIG. 1(a) shows a top perspective view of a semiconductor package according to an embodiment of the invention.

[0011] FIG. 1(b) shows a bottom perspective view of the package in FIG. 1(a).

25 **[0012]** FIG. 1(c) shows a side cross-sectional view of the semiconductor package in FIGS. 1(a) and 1(b) mounted on a circuit substrate.

[0013] FIG. 1(d) shows a package configuration with only one die.

[0014] FIG. 2 shows a package configuration with two dies.

[0015] FIG. 3(a) shows a top perspective view of the package according to another embodiment of the invention.

[0016] FIG. 3(b) shows a bottom perspective view of the package in FIG. 3(a).

5 **[0017]** FIG. 3(c) shows a top perspective view the package in FIG. 3(a) with a heat plate structure.

[0018] FIG. 3(d) shows a side cross-sectional view of the package in FIGS. 3(a) and 3(b).

10 **[0019]** FIGS. 4(a)-4(e) show various illustrations of a package as it is being formed.

[0020] FIG. 5 shows an exploded view of a package according to an embodiment of the invention.

[0021] These and other embodiments are described in further detail below in the Detailed Description.

15 **DETAILED DESCRIPTION**

[0022] Embodiments of the invention are directed to an alternative design and method of manufacture for an FLMP package. In embodiments of the invention, mechanical stress experienced by a semiconductor die during a molding process is substantially eliminated. As indicated above, mechanical stress during the process of manufacturing a package can lead to die cracking or solder cracking. Embodiments of the invention also eliminate the possibility of mold bleed or mold resin contamination on an exposed backside of a die. Using embodiments of the invention, it is possible to create thinner packages (*e.g.*, less than about 0.5 mm in height) where it is difficult to do so in a standard FLMP manufacturing method. In some
20
25
embodiments, an opening at the top surface of the package also provides for optional use of an additional heat sink such as a heat plate structure to provide for better thermal dissipation.

[0023] The semiconductor package may use a pre-plated and/or pre-formed copper based leadframe structure, a pre-molding technique that produces a premolded leadframe structure, a solder bumped or non-solder bumped semiconductor die, and an intermediate solder paste. The details and benefits of using each of these features are explained below.

[0024] First, copper is an excellent electrical and thermal conductor so copper leadframe structures are preferred in embodiments of the invention. In some embodiments, the leadframe structure may be preplated with metals such as NiPdAu. Pre-plating the leadframe structure reduces the package's exposure to chemicals, since the finished package need not be exposed to chemicals such as plating chemicals after it is formed. Pre-plating a leadframe structure also allows one to subject the leadframe structure to high reflow temperatures without melting. Pre-forming the leadframe structure also eliminates the mechanical stresses to be absorbed by the package due to the leadforming process.

[0025] Second, a pre-molding technique may be used to form a pre-molded leadframe structure in embodiments of the invention. The premolded leadframe structure is a desirable feature of embodiments of the invention. In the premolded leadframe structure, the leadframe structure and the molding material can be locked together. The premolded leadframe structure can provide for an exposed leadframe surface for die attachment without using any film or tape. It is possible to maintain die backside planarity with respect to the exposed leads of the leadframe structure depending on the package configuration for the drain, gate and source connections to the circuit substrate (*e.g.*, a PC board). The premolded leadframe structure includes a first window for receiving a die, and an optional second window for receiving a heat sink such as a heat plate structure (for further thermal dissipation).

[0026] Third, an array of bumps in the die may serve as the source and gate electrical terminals for a transistor die. They also serve as mechanical and thermal stress absorbers between the die and the leadframe structure. In the conventional FLMP package, the bumps are tall so that enough space is provided for a molding material to flow between the silicon die and the leadframe structure. A soft solder bump material is also ideal for a standard FLMP package to minimize the compression stress that is absorbed by the die during the molding process. In

comparison, in embodiments of the invention, any bump material and shorter heights can be used, since molding is performed before die attachment to the leadframe structure. The materials and heights of the bumps are independent of molding process considerations.

5 **[0027]** In embodiments of the invention, the package can use silicon dies with thicknesses down to 0.10 mm. Also, solder paste is used to couple the bumps on a die (especially for non-solder bumps) to the leadframe structure to provide for an electrical and mechanical connection. The bumps, and solder paste can be Pb-based or Pb-free solder materials, with melting temperatures above 260 °C in some
10 embodiments. The bumps can comprise a non-solder material like copper and gold.

[0028] Embodiments of the invention also provide for leadframe structure variations to meet desired electrical pin-out configurations and to allow for multiple dies in a single package. Embodiments of the invention also provide for a top window opening in the molding material to provide for a heatsink option. In some
15 embodiments, it is also possible to use a thinner leadframe structure, a thinner molding material, a thinner die, and shorter bumps so that a package that is 0.50 mm or less in thickness can be produced.

[0029] FIG. 1(a) shows a package **100** according to an embodiment of the invention. The package **100** includes a molding material **22** with two holes **20** at the
20 top of the package **100**. The holes **20** may be provided to allow for better thermal dissipation from the die that is in the package **100**. Any suitable molding material **22** including, for example, an epoxy molding material may be used. The package **100** also includes a number of leads **24** including a gate lead **24(g)** and a plurality of source leads **24(s)**. The illustrated package **100** has 7 source leads and one gate lead.
25 Other package embodiments may have more or less leads.

[0030] The leads **24** in the package **100** may be part of a leadframe structure. As used herein, the term “leadframe structure” can refer to a structure that is derived from a leadframe. A typical leadframe structure includes a source lead structure, and a gate lead structure. Each of the source lead structure and the gate lead structure can
30 have one or more leads.

[0031] FIG. 1(b) shows a bottom side view of the package 100. The package 100 includes a semiconductor die 30. A backside 30(a) of the semiconductor die 30 may show through a window in the molding material 22. The backside 30(a) of the die 30 corresponding to the drain region of a transistor in the die 30 may be metallized and may be distal to a die attach region of the leadframe structure. The opposite frontside of the die 30 may correspond or include a source region and a gate region and may be proximate to the die attach region of the leadframe structure. The die backside 30(a) provides for an electrical terminal, and may be coplanar with the bottom surface of the molding material 22 and coplanar with the ends of the leads 24. The window in the molding material 22 is slightly larger than the outer edges (and planar dimensions) of the die 30.

[0032] A small gap 11 is present between the molding material 22 and the outer edges of the die 30. This small gap 11 also allows the die 30 to thermally expand and contract independently of the molding material 22. As shown, the gap 11 may extend around the entire periphery of the die 30. No molding material is present between the solder joints coupling the leadframe structure and the die 30.

[0033] FIG. 1(c) shows a side cross-sectional view of an electrical assembly 103. The package 100 shown in FIGS. 1(a) and 1(b) is mounted on a circuit substrate 55 in FIG. 1(c). Solder (not shown) such as 63Sn/37Pb may be used to electrically couple the backside of the die 30 and the ends of the leads 24 to one or more conductive regions in the circuit substrate 55. As shown therein, a small gap 11 is present between the molding material 22 and the outer edges of the die 30.

[0034] FIG. 1(d) shows the leadframe structure 38. Bumps 34 are also shown attaching the die 30 to the leadframe structure 36. Apertures 38 may be present in the leadframe structure 36 to allow a molding material 22 to flow through and lock to the leadframe structure 36.

[0035] The semiconductor dies used in the semiconductor packages according to preferred embodiments of the invention include vertical power transistors. Vertical power transistors include VDMOS transistors. A VDMOS transistor is a MOSFET that has two or more semiconductor regions formed by diffusion. It has a source region, a drain region, and a gate. The device is vertical in that the source region and

the drain region are at opposite surfaces of the semiconductor die. The gate may be a
trenched gate structure or a planar gate structure, and is formed at the same surface as
the source region. Trenched gate structures are preferred, since trenched gate
structures are narrower and occupy less space than planar gate structures. During
operation, the current flow from the source region to the drain region in a VDMOS
device is substantially perpendicular to the die surfaces.

[0036] FIG. 2 shows a package 101 with two semiconductor dies 30(a), 30(b)
and two corresponding leadframe structures 36(a), 36(b) within a single molding
material. Each leadframe structure 36(a), 36(b) includes a gate lead and a plurality of
source leads. Apertures 38 are in the die attach regions of the leadframe structures
36(a), 36(b). In other embodiments, there could be even more leadframe structures
and even more dies per package.

[0037] FIG. 3(a) shows a top view of another embodiment of the invention.
The package 100 includes a top window 58 in a molding material 22 that exposes the
top surface 24(x) of a leadframe structure 24. The top surface 24(x) may be the
surface that is opposite to the surface to which the die is attached.

[0038] FIG. 3(b) shows a bottom side view of the package 100 shown in FIG.
3(a). The package 100 includes a die 30 that is in another window in the molding
material 22. As shown, the backside 30(a) of the die is exposed through the molding
material 22. Thus, the package 100 may have first and second windows at opposite
sides of the package 100.

[0039] FIG. 3(c) shows a metal plate structure 52 that is coupled to the top
surface 24(x) of the leadframe structure 24. As shown, the metal plate structure 52
has a first portion that is planar and is coupled to the top surface 24(x) of the
leadframe structure and has a leg that extends down the side of the package 100. The
leg of the metal plate structure 52 may provide for an additional electrical and/or
thermal connection for the package 100 to an underlying circuit substrate (not shown).

[0040] FIG. 3(d) shows a side cross-sectional view of the package 100,
without a metal plate structure. As shown, a gap 15 is presented between the outer
edges of the die 30 and the molding material 22. As shown, the bottom surface of the
molding material 22 is coplanar with the die backside 30(a) and the ends of the leads

24(s). Also, as shown in FIG. 3(d), there is no molding material between the joints coupling the leadframe structure and the die **30**.

[0041] The above-described embodiments may be manufactured in any suitable manner. For example, a first process flow option may include the following processes: 1. pre-mold/degate/deflash processes, 2. a water jet deflash process, 3. solder dispense/flipchip attach processes, and 4. a reflow process. The reflow process may be followed by: A. leadcut/test/mark processes, and B. singulate/tape and reel processes. The reflow process may alternatively be followed by singulate/test/mark/tape and reel processes. In another example, a second process flow option is as follows: 1. pre-mold/degate/deflash/leadcut processes, 2. solder dispense/flipchip attach processes, and 3. a reflow process. The reflow process may be further followed by A. a test/mark process, and B. singulate/tape and reel processes. The IR reflow process may alternatively be followed by singulate/test/mark/tape and reel processes. These individual processes are known to those of ordinary skill in the art.

[0042] Referring to FIGS. 4(a) to 4(e), the first step is to mold the molding material **22** onto the leadframe structure **24**. Referring to FIG. 4(a), the leadframe structure **24** is loaded into a mold tool **60** with a cavity designed to meet the intended predefined package thickness, form and leadframe exposure. A molding material is allowed to liquify, and enters the mold cavity and solidifies between the molding dies of the mold tool **60**. After molding, the formed molded strip (if the leadframe is one of many leadframes in a strip of leadframes) goes through a degate/deflash process to remove the excess mold on the leads or leadframe structures. If the molded strip requires further cleaning, the molded strip can undergo a water jet deflash process. If no further cleaning is required, one process option is to completely cut all extended leads leaving the tiebars connected to the sides of the die attach pads of the leadframe structures. This can be done prior to the attachment of the semiconductor dies to the leadframe structures.

[0043] A molded leadframe structure **99** is shown in FIG. 4(b) and includes a molding material **22** and a leadframe structure. As shown, a relatively large window **98** for receiving a die is in the molding material **22**. The window **98** exposes the die attach region **97** of the leadframe structure **24**.

[0044] Referring to FIG. 4(c), a solder dispensing process and a flip chip attach process may be performed. The bump **34(a)** comprising, for example, 95Pb/5Sn may be deposited on the die **30** in a first array. The solder material **34(b)** comprising, for example, 88Pb/10Sn/2Ag may be deposited on the exposed surface of the die attach region of the leadframe structure **24** in a second array. The bump material **34(a)** may have a higher melting temperature than the solder paste material **34(b)**. (The solder that is used to attach the finished package to a circuit substrate may have a lower melting temperature than either the bump or the solder paste materials.) As shown in FIG. 4(c), the bumped die **30** is flipped over and the arrays of bumps and solder paste materials **34(a)**, **34(b)** are aligned and joined to form an array of joints joining the leadframe structure **24** and the die **30**. As shown, the semiconductor die **30** fits within the window in the molding material **22** and a small gap is between the die **30** and the edges of the window in the molding material **22**. The backside of the die **30** does not have any residual molding material, since the molding process was already performed.

[0045] As shown in FIG. 4(d), after the die is attached to the leadframe structure, the combination goes to a reflow oven to melt the solder paste and cohesively attach the bumped silicon die to the pre-molded leadframe. Suitable reflow temperatures can be chosen by those of skill in the art.

[0046] Referring to FIG. 4(e) and 4(f), electrical testing and further processing can be done. A first approach is to perform strip testing and marking before performing singulation and then tape and reel processes. If the leads are still not cut, lead cutting can be done prior to strip testing. The second approach is to perform leadcut and singulation processes first, and then to do unit testing and marking before performing a tape and reel process. FIG. 4(f) shows a package in a tape and reel process.

[0047] FIG. 5 shows an exploded view of a package. As shown, the package includes a molding material **22** that is coupled to a leadframe structure **24**. A semiconductor die **30** with an array of bumps **34(a)** is coupled to the leadframe structure **24** with a solder paste material **34(b)**.

[0048] It is noted that the present invention is not limited to the preferred embodiments described above, and it is apparent that variations and modifications by those skilled in the art can be performed within the spirit and scope of the present invention. Moreover, any one or more embodiment of the invention may be
5 combined with one or more embodiments of the invention without departing from the spirit and scope of the invention.

[0049] All U.S. provisional and non-provisional patent applications and publications mentioned above are incorporated by reference in their entirety for all purposes.